Claims

What is claimed is:

1. A serial peripheral interface apparatus, comprising:

a plurality of serial data-transfer means coupled together for transferring data serially;

buffer means coupled to said plurality of serial data-transfer means for storing a subsequent data byte to be transferred;

counter means coupled to said buffer means and said plurality of serial data-transfer means for checking a status of a data transmission within said apparatus; and

control means coupled to said buffer means, said counter means, and said plurality of data transferring means for controlling said data transmission within said apparatus and for enabling a loading of said subsequent data byte into said buffer means by reviewing a status of said counter means and a status of said buffer means.

2. The serial peripheral interface apparatus of claim 1, wherein a plurality of serial data-transfer means further comprises a first serial data-transfer means serving as a serial master with an output coupled to a second serial data-transfer means serving as a serial slave.

3. The serial peripheral interface apparatus of claim 2, wherein said first serial data-transfer means further comprises a multiplexer means coupled to a latching means.

4. The serial peripheral interface apparatus of claim 2, wherein said second serial data-transfer means further comprises a multiplexer means coupled to a latching means.

5. The serial peripheral interface of claim 1 further comprising a parallel data-transfer means serving as a parallel slave, the parallel data-transfer means coupled to an output of one of said serial data-transfer means.

6. The serial peripheral interface apparatus of claim 5, wherein said parallel slave data-transfer means further comprises a latching means.

7. The serial peripheral interface apparatus of claim 1, wherein said control means further controls a loading of said subsequent data byte to said plurality of serial data-transfer means.

8. The serial peripheral interface apparatus of claim 1, wherein the control means is responsive to the status of the counter means for permitting loading of data bytes into said buffer means only until a time slot in which a fourth bit of a present data byte is transferred.

9. A serial peripheral interface apparatus, comprising:

a plurality of shift registers coupled together for transferring data serially;

a write buffer coupled to said plurality of shift registers;

a bit counter coupled to said plurality of shift registers for keeping track of a bit field of a data byte being transferred through said apparatus; and

a finite state machine controller coupled to said apparatus for controlling data transmission therethrough and for enabling a loading of a subsequent data byte into said write buffer by checking a status of said bit counter and a status of said write buffer.

10. The apparatus of claim 9, wherein said plurality of shift registers further comprises a serial master shift register, a serial slave shift register coupled to an output of said serial master shift register for transferring data serially, and a parallel slave shift register coupled to said output of said serial master shift register.

11. The serial peripheral interface apparatus of claim 10, wherein said master serial shift register further comprises a multiplexer coupled to a clocked flip-flop.

12. The serial peripheral interface apparatus of claim 10, wherein said serial slave shift register further comprises a multiplexer coupled to a clocked flip-flop.

13. The serial peripheral interface apparatus of claim 10, wherein said parallel slave shift register further comprises a clocked flip-flop.

14. The serial peripheral interface apparatus of claim 10, wherein said finite state machine controller further controls a loading of said data byte to said plurality of shift registers.

15. The serial peripheral interface apparatus of claim 10 wherein the finite state machine controller is responsive to a status of the bit counter so as to permit loading of a subsequent data byte into the write buffer only until a time slot in which a fourth bit of a present data byte is transferred.

16. A microcontroller comprising:

a central processing unit;

a bus interface coupled to said central processing unit;

a memory module coupled to and in communication with said central processing unit via said bus interface;

a serial peripheral interface module coupled to said memory module and said bus interface; said serial peripheral interface further comprising:

a serial master shift register, a serial slave shift register coupled to an output of said serial master shift register for transferring data serially, and a parallel slave shift register coupled to said output of said serial master shift register;

a write buffer coupled to said input of said serial slave shift register;

a bit counter coupled to said serial peripheral interface module for keeping track of a data set being transferred therethrough; and

a finite state machine controller coupled to said serial peripheral interface module for controlling data transmission therethrough and for enabling a loading of a subsequent data byte into said write buffer by providing the status of said bit counter and a status of said write buffer back to said central processing unit.